D. Remarks

Rejection of Claims 1, 3, 5-7, 9 and 11 Under 35 U.S.C. §102(e) or §103(a) based on U.S. Patent No. 6,242,323 (*Ishitsuka et al.*).

The rejection of claims 1, 3 and 5 will first be addressed.

The invention of amended claim 1 is directed to a semiconductor device that includes a trench element separation region including a trench formed in a surface of a semiconductor substrate. An oxide film is formed on inner walls of the trench.

A trench filling insulating material fills the trench and has edges above the inner walls of the trench. Inner wall edges in a top section of the trench and edges of the trench filling insulating material are formed to be essentially located on the same plane when viewed in cross section. Further, the edges of the trench filling material are defined by side edges of a sacrificial layer formed by a pullback etching process including a neutral radical performed for the trench filling process.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.[1] Alternatively, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

The cited reference *Ishitsuka et al.* does not show a trench filling material with edges defined by side edges of a sacrificial layer, as recited in amended claim 1. This particular edge structure has nonobvious differences over the conventional approach of *Ishitsuka et al.* As evidence in support of such differences, Applicant submits the following:

1. Appendix A: Applicant's Experimental Results (Table 1 of the Specification)
2. Appendix B: Applicant's Etch Amount versus Etch Time Results (FIGS. 4 and 5)

Appendix A

[1] See Lindemann Maschinenefabrick GmbH v. American Hoist & Derrick Col., 221 USPQ 481, 485 (Fed. Cir. 1984).

Appendix A shows superior controllability results that can be obtained with Applicant's invention. That is, Appendix A shows that the position of the side edges of the sacrificial layer may be set with better accuracy than conventional approaches. By controlling etching amount in such away, superior transistor threshold voltages can be achieved.[2]

Appendix B

Appendix B shows a comparison between conventional etch results (FIG. 5) versus that according to an embodiment of the present invention (FIG. 4). As shown in the figures, failure to utilize Applicant's neutral radical etching back approach results in "etching inoperative times"[3] dependent upon an oxidized thickness of a sacrificial layer. That is, Appendix B shows how the present invention eliminates imprecision in the position of side edges of the sacrificial layer.

In summary, Applicant's claim 1 recites side edges of a sacrificial layer formed by a pullback etching process including a neutral radical performed in a trench filling process. Such side edges have the nonobvious difference of more precise edge placement. This translates into a more precise position for the edges of the trench filling insulating material. Still further, when utilized in conjunction with transistors, such a feature results in reduced variation in transistor threshold voltages.

In summary, Applicant's experimental results present a structure with nonobvious, advantageous features over conventional approaches. Further, because such features are absent from the cited art, anticipation or a prima facie case of obviousness cannot have been established for claim 1, and this ground for rejection claim 1 is traversed.

The rejection of claims 7, 9 and 11 will now be addressed.

Claim 7 is directed to a semiconductor device having a trench element separation region with a trench that separates a first doped channel of a first insulated gate field effect transistor (IGFET) from a second doped channel of a second IGFET. An oxide is formed on inner walls of the trench.

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[2] See the Specification, FIG. 8, which indicates that controlling a pullback etching amount to 20 nm or less, produces limited variation in a resulting transistor threshold.

[3] See the Specification, Page 19, Lines 2-9.

A trench filling insulating material fills the trench and has edges above the inner walls of the trench. Inner wall edges in a top section of the trench and edges of the trench filling insulating material are formed to be essentially located on the same plane when viewed in cross section. Further, the edges of the trench filling material are defined by side edges of a sacrificial layer formed by a pullback etching process including a neutral radical performed before filling the trench.

To address this ground of rejection, Applicant incorporates by reference the remarks set forth above for claim 1. Namely, that the claim includes nonobvious and advantageous features and results over conventional approaches.

Further, it is emphasized that the above semiconductor device has less variability in threshold voltage, as compared to conventional approaches. In support of such a nonobvious difference, Applicant submits Appendix C, which shows how variability in threshold voltages (Vts) can result, absent precise etching amounts.

Rejection of Claims 7, 9 and 11 Under 35 U.S.C. §102(e) or §102(e) based on U.S. Patent No. 6,258,697 (*Bhakta et al.*).

The cited reference *Bhakta et al.* does not show "edges of the trench filling material are defined by side edges of a sacrificial layer", as recited in claim 7.

In *Bhakta et al.*, as shown in FIGS. 3C and 3D, edges of a trench filling material 46 (argued to correspond to Applicant's trench filling material) are defined by oxide liner 42 not polish stop layer 34 (argued to correspond to Applicant's sacrificial layer). Thus, the reference does not show or suggest all limitations of claim 7. Accordingly, anticipation or a prima facie case of obviousness has not been established for this claim.

For this reason alone, this ground of rejection is traversed.

In addition or alternatively, to address this ground of rejection Applicant's incorporate by reference herein the comments set forth above for claim 1. Namely, that Applicant's limitation of "edges of the trench filling material are defined by side edges of a sacrificial layer formed by a pullback etching process including a neutral radical performed in a trench filling process" is neither shown nor suggested by the cited reference. Further, such a limitation has patentable weight due to nonobvious differences arising from the resulting edge structure.

Claims 1 and 7 have been amended, not in response to the cited art, but to clarify particular claim limitations.

The present claims 1, 3, 5-7 and 9-11 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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APPENDIX A

	Liner Oxide Film Etching Amount
Present Invention (1)	1/3
Present Invention (2)	1/5
Conventional Method	1 (for example 9 nm)

Applicant's Table 1.

APPENDIX B

FIG. 4

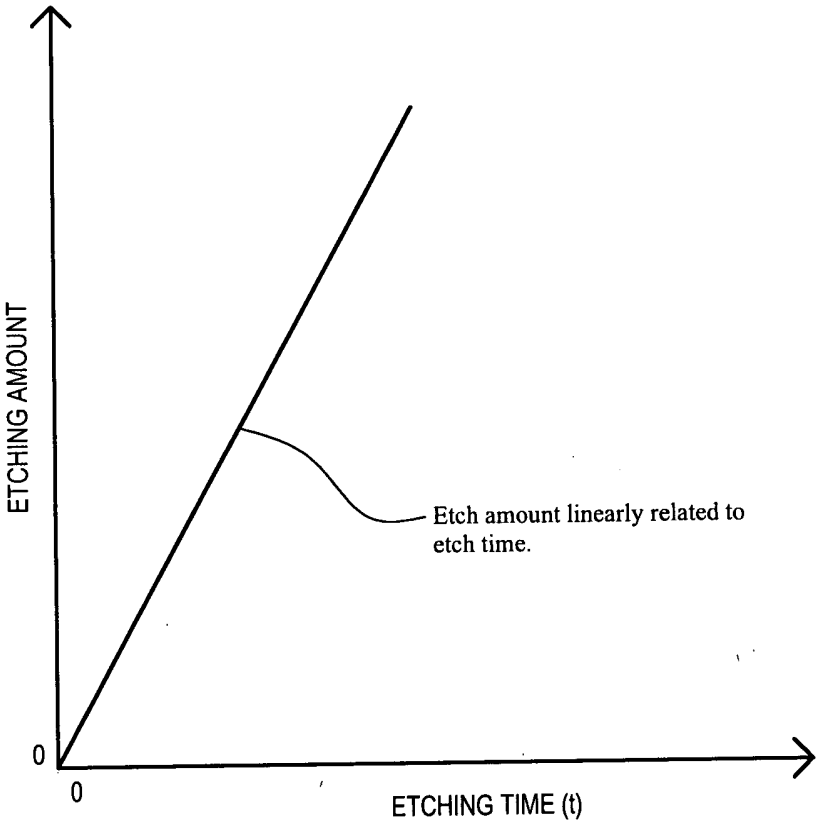
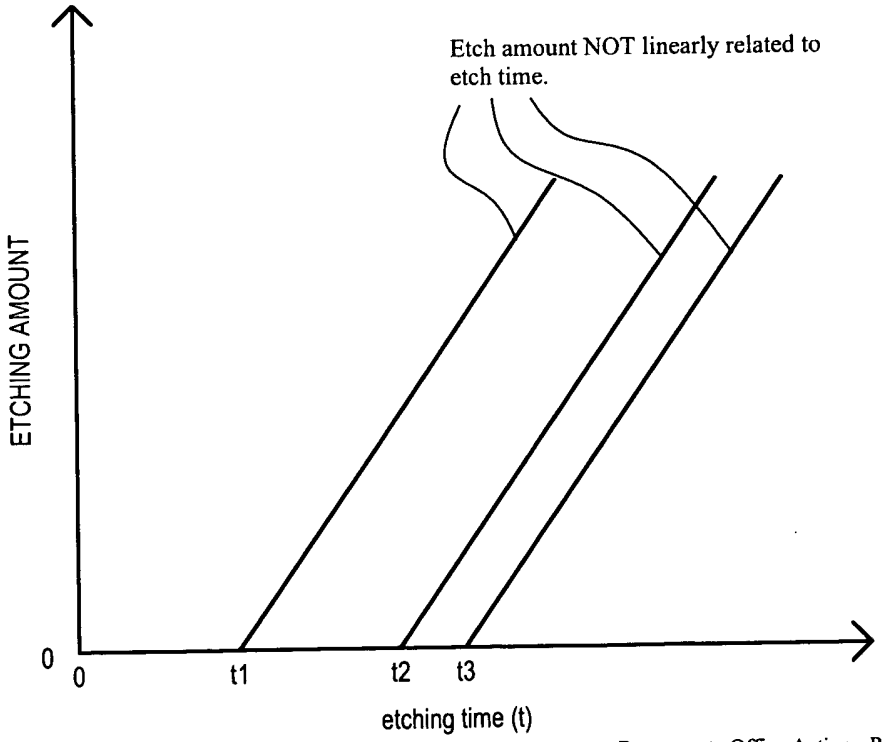


FIG. 5



APPENDIX C

FIG. 8